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| EXAMINER | |
|---|---|
| SPITTLE, MATTHEW D | |

| ART UNIT | PAPER NUMBER |
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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/717,177 | PEZZINI, SAVERIO | |
| | Examiner | Art Unit | |
| | Matthew D. Spittle | 2111 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *10-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10,11,13-17 and 19-30* is/are rejected.

7)☒ Claim(s) *12 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Response to Arguments*

Regarding applicant's traversal of Khan, Examiner agrees that Khan et al. fails to disclose priority counters as in the claimed invention. Oman et al., however, teach a plurality of counters which, when used as taught, would reduce arbitration overhead and the burden on the microprocessor. Therefore, Examiner finds reason to combine Khan et al. with Oman et al.

In response to applicant's argument that the priority counters of Oman et al. are directed to the use of LAN networks and not interrupt controllers - a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Regarding applicant's traversal of Manber et al., Examiner agrees that Manber et al. uses a more complicated function to cancel an interrupt and its priority from pending and priority registers after having been processed than that of the claimed invention. Given the broadest reasonable interpretation of the claim in addition to what is well known in the art, Examiner finds Manber et al. to meet this limitation.

Regarding applicant's traversal of Norman et al., applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "the actions to be carried out depend on the

corresponding interrupt request") are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Regarding applicant's traversal of Chou et al, applicant's argument that Chou et al. is directed toward destination processors with a different circuit and function - a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Therefore, Examiner cannot allow claims 10 – 30.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

Determining the scope and contents of the prior art.
Ascertaining the differences between the prior art and the claims at issue.
Resolving the level of ordinary skill in the pertinent art.

Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. in view of Oman et al., and further in view of Manber et al.

With regard to claim 10, Khan et al teach a method for generating interrupts for a microprocessor system, the method comprising:

Storing interrupts in a pending interrupts register (Figure 2, item 142; column 8, lines 28 – 30).

Storing priority values associated with the stored interrupts in a plurality of priority registers (Figure 4, item 300) coupled to the pending interrupts register (Figure 2, item 142; column 12, lines 65 – 66).

Comparing the priority values for identifying the interrupt having the highest priority if an interrupt service routine is not being executed (column 10, lines 55 – 59).

Processing the interrupt having the highest priority by generating an interrupt command and an interrupt vector identifying the interrupt service routine to be executed (column 3, lines 52 – 63; column 9, lines 5 – 18).

However, Khan et al fail to teach a plurality of counters which increment priority values stored therein at predetermined intervals.

Oman et al. teach loading a plurality of counters with starting priority values (column 14, lines 3 – 5, 16 – 27).

Oman et al. teach incrementing at predetermined intervals the priority values loaded in a plurality of counters (column 2, lines 31 – 42; claim 1(c)).

Neither Khan et al. or Oman et al. teach canceling the interrupt having the highest priority from the pending interrupts register and its priority value from the plurality of priority registers. This step is necessarily inherent in the design of any arbitration mechanism where fairness is a requirement. Manber et al. describes the process of inhibiting an "agent's" right to compete for arbitration after winning access to a resource until all other "agents" have also been served (column 3, lines 30 – 36, 46 – 53). Examiner identifies this as being equivalent to canceling an interrupt and its priority from the pending and priority registers respectively after having been processed.

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the method of Khan et al to incorporate the plurality of priority counters as taught by Oman et al. in order to provide for a means of fairness in processing interrupts. This would have been obvious since Oman et al. teach that using counters in the method taught reduces arbitration overhead, as well as the burden on the microprocessor (column 16, lines 43 – 48).

Claims 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. in view of Oman et al., in view of Manber et al., and further in view of Norman et al.

With regard to claim 11, Khan et al., and Oman et al. fail to teach incrementing each counter wherein the incrementing is based upon increment signals having different periods. Norman et al. teach incrementing priority values at different periods that may be fixed or variable (paragraphs 176, 182).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the method of Khan et al., and Oman et al., to incorporate the method of Norman et al. of incrementing the priority values of each interrupt according to different periods in order to provide an aging policy for said interrupts (paragraphs 176 – 178, 181 – 185).

Claims 13, 14, 15, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. in view of Oman et al., and further in view of Manber et al.

With regard to claim 13, Khan et al. teach the additional limitation of the method of claim 10 comprising the following for managing nested interrupts:

Storing the priority value of the interrupt being processed in a memory buffer (Figure 2, item 172; column 4, lines 16 – 21; column 10, lines 52 – 55).

Comparing the priority values stored in the plurality of counters with the priority value stored in the memory buffer for identifying a new interrupt having the highest priority (column 10, lines 55 – 59).

If the new interrupt has the highest priority, then stopping execution of the interrupt service routine and storing in a stack register (Figure 2, item 162) the priority value corresponding to the interrupt service routine whose execution was stopped (column 10, lines 49 – 51; column 9, line 60 – column 10, line 9; column 10, lines 48 – 51; column 14, lines 58 – 64).

Generating a new interrupt command and a new interrupt vector for identifying a new interrupt service routine to be executed based upon the new interrupt having the highest priority (column 3, lines 52 – 63; column 9, lines 5 – 18).

Khan et al. fail to explicitly state canceling the priority value from the stack register corresponding to the interrupt service routine whose execution was stopped. However, examiner assumes applicant means to refer to the priority value corresponding to the interrupt service routine which was processed. In this case, this step is inherently present in the system of Khan et al. (column 11, lines 17 – 21).

With regard to claim 14, Khan et al. teach a method for generating interrupt commands for a microprocessor system, the method comprising:

Storing interrupts in a pending interrupts register (Figure 2, item 142; column 8, lines 28 – 30).

Storing priority values associated with the stored interrupts in a plurality of priority registers (Figure 4, item 300) coupled to the pending interrupts register (Figure 2, item 142; column 12, lines 65 – 66).

Processing the interrupt having the highest priority by generating an interrupt command and an interrupt vector identifying the interrupt service routine to be executed (column 3, lines 52 – 63; column 9, lines 5 – 18).

Khan et al. fail to teach loading a plurality of counters coupled in cascade to the plurality of priority registers with the stored priority values, and then incrementing the said priority values at predetermined intervals.

Oman et al. teach loading a plurality of counters with starting priority values (column 14, lines 3 – 5, 16 – 27).

Oman et al. teach incrementing at pre-determined intervals the priority values loaded in a plurality of counters (column 2, lines 31 – 42; claim 1(c)).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the method of Khan et al to incorporate the plurality of priority counters as taught by Oman et al. in order to provide for a means of fairness in processing interrupts. This would have been obvious since Oman et al. teach that using counters in the method taught reduces arbitration overhead, as well as the burden on the microprocessor (column 16, lines 43 – 48).

With regard to claim 15, Khan et al. teach the additional limitation of processing the interrupt having the highest priority comprising generating a new interrupt command and an interrupt vector for identifying a new interrupt service routine to be executed (column 3, lines 52 – 63; column 9, lines 5 – 18).

With regard to claim 19, Khan et al. teach the additional limitation of a method according to claim 15, further comprising performing the following for managing nested interrupts:

Storing the priority value of the interrupt being processed in a memory buffer (Figure 2, item 172; column 4, lines 16 – 21; column 10, lines 52 – 55).

Comparing the priority values stored in the plurality of counters with the priority value stored in the memory buffer for identifying a new interrupt having the highest priority (column 10, lines 55 – 59).

If the new interrupt has the highest priority, then stopping execution of the interrupt service routine and storing in a stack register (Figure 2, item 162) the priority value corresponding to the interrupt service routine whose execution was stopped (column 9, line 60 – column 10, line 9; column 10, lines 48 – 51; column 14, lines 58 – 64).

Generating a new interrupt command and a new interrupt vector for identifying a new interrupt service routine to be executed based upon the new interrupt having the highest priority (column 3, lines 52 – 63; column 9, lines 5 – 18).

Khan et al. fail to explicitly state canceling the priority value from the stack register corresponding to the interrupt service routine whose execution was stopped. However, examiner assumes applicant means to refer to the priority value corresponding to the interrupt service routine which was processed. In this case, this step is inherently present in the system of Khan et al. (column 11, lines 17 – 21).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. in view of Oman et al., and further in view of Manber et al.

Neither Khan et al. or Oman et al. teach canceling the interrupt having the highest priority from the pending interrupts register and its priority value from the

plurality of priority registers. This step is necessarily inherent in the design of any arbitration mechanism where fairness is a requirement.

Manber et al. teach the process of inhibiting an "agent's" right to compete for arbitration after winning access to a resource until all other "agents" have also been served (column 3, lines 30 – 36, 46 – 53). Examiner identifies this as being equivalent to canceling an interrupt and its priority from the pending and priority registers respectively after having been processed.

Claims 17 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. in view of Oman et al., in view of Manber et al., and further in view of Norman et al.

With regard to claim 17, Khan et al., and Oman et al. fail to teach incrementing each counter wherein the incrementing is based upon increment signals having different periods. Norman et al. teach incrementing priority values at different periods that may be fixed or variable (paragraphs 176, 182).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the method of Khan et al., and Oman et al., to incorporate the method of Norman et al. of incrementing the priority values of each interrupt according to different periods in order to provide an aging policy for said interrupts (paragraphs 176 – 178, 181 – 185).

Claims 20, 21, 24 – 27, and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. in view of Chou et al, and further in view of Oman et al.

With regard to claim 20, Khan et al. teach a control circuit for generating interrupt commands for a microprocessor system comprising:

A pending interrupts registers for storing interrupts (Figure 2, item 142; column 8, lines 28 – 30).

A plurality of priority registers (Figure 4, item 300) coupled to said pending interrupts register for storing priority values associated with the stored interrupts (Figure 2, item 142; column 12, lines 65 – 66).

Khan et al. fail to teach loading a plurality of counters coupled in cascade to the plurality of priority registers with the stored priority values, and then incrementing the said priority values at predetermined intervals. Khan et al. also fail to teach a priority comparing circuit and a logic processing circuit as described by the applicant.

Oman et al. teach loading a plurality of counters coupled in cascade to said plurality of priority registers and being loaded with the stored priority values, the stored priority values being incremented at predetermined intervals (column 14, lines 3 – 5, 16 – 27; column 2, lines 31 – 42; claim 1(c)).

Chou et al. teach a priority comparing circuit coupled to a pending interrupts register for identifying the interrupt having a highest priority if an interrupt service routine is not being executed, and generating an interrupt request signal and an internal signal corresponding to the interrupt having the highest priority stored in said pending

interrupts register (figure 10; column 3, lines 4 – 7; column 4, lines 46 – 51; column 5, lines 13 – 19; column 7, lines 4 – 13; column 11, lines 8 – 11, lines 28 – 30).

Chou et al. teach a logic processing circuit (figure 6) coupled to said priority comparing circuit and receiving the interrupt request signal and the internal signal, and generating for the microprocessor system an interrupt command and an interrupt vector identifying an interrupt service routine to be executed (column 5, lines 26 – 57).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuit of Khan et al. to include a plurality of counters being loaded with priority values which are incremented at predetermined intervals to provide for a means of fairness in processing interrupts. This would have been obvious since Oman et al. teach that using counters in the method taught reduces arbitration overhead, as well as the burden on the microprocessor (column 16, lines 43 – 48).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuit of Khan et al. and Oman et al. to include a priority comparing circuit as taught by Chou et al. in order to identify the highest priority interrupt (column 11, lines 47 – 50).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuit of Khan et al. and Oman et al. to include a logic processing circuit as taught by Chou et al in order to receive the interrupt request signal, and generate the interrupt command and interrupt vector that identifies the interrupt service routine to be executed (column 5, lines 47 – 57).

With regard to claim 21, Oman et al. teach the additional limitation of a control circuit where a plurality of counters receives increment signals from a system clock signal (column 13, line 17, lines 35 – 37, lines 41 – 46).

With regard to claim 24, Khan et al. teach the additional limitation of a control circuit wherein the interrupts are nested, and wherein said logic processing circuit comprises:

A memory buffer coupled to said priority comparing circuit for storing the priority vale of the interrupt being represented by an internal signal (column 10, lines 52 – 64).

A stack register coupled to a memory buffer for storing the priority value corresponding to the interrupt service routine whose execution was stopped because of a new interrupt having a higher priority value (column 14, lines 58 – 64).

With regard to claim 25, Khan et al. teach a microprocessor system comprising:

A microprocessor (column 3, lines 23 – 33).

A control circuit for generating interrupt commands for said microprocessor, said control circuit comprising:

A pending interrupts register for storing interrupts (Figure 2, item 142; column 8, lines 28 – 30).

A plurality of priority registers coupled to said pending interrupts register for storing priority values associated with the stored interrupts (Figure 4, item 300) coupled to the pending interrupts register (Figure 2, item 142; column 12, lines 65 – 66).

Oman et al. teach a plurality of counters coupled in cascade to said plurality of priority registers and being loaded with the stored priority values, the stored priority values being incremented at predetermined intervals (column 14, lines 3 – 5, 16 – 27; column 2, lines 31 – 42; claim 1(c)).

Chou et al. teach a priority comparing circuit coupled to said plurality of counters and to said pending interrupts register for comparing the incremented priority values for identifying the interrupt having a highest priority (Figure 10; column 3, lines 4 – 7; column 4, lines 46 – 51; column 5, lines 13 – 19; column 7, lines 4 – 13; column 11, lines 8 – 11, lines 28 – 30).

Chou et al. teach a logic processing circuit (figure 6) coupled to said priority comparing circuit and generating for said microprocessor an interrupt command and an interrupt vector identifying an interrupt service routine to be executed (column 5, lines 26 – 57).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuit of Khan et al. to include a plurality of counters being loaded with priority values which are incremented at predetermined intervals to provide for a means of fairness in processing interrupts. This would have been obvious since Oman et al. teach that using counters in the method taught reduces

arbitration overhead, as well as the burden on the microprocessor (column 16, lines 43 – 48).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuit of Khan et al. and Oman et al. to include a priority comparing circuit as taught by Chou et al. in order to identify the highest priority interrupt (column 11, lines 47 – 50).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the circuit of Khan et al. and Oman et al. to include a logic processing circuit as taught by Chou et al in order to receive the interrupt request signal, and generate the interrupt command and interrupt vector that identifies the interrupt service routine to be executed (column 5, lines 47 – 57).

With regard to claim 26, Chou et al. teach the additional limitation of a microprocessor system wherein a priority comparing circuit generates an interrupt request signal and an internal signal representing the interrupt having the highest priority stored in said pending interrupts register (figure 10; column 3, lines 4 – 7; column 4, lines 46 – 51; column 5, lines 13 – 19; column 7, lines 4 – 13; column 11, lines 8 – 11, lines 28 – 30); and wherein said logic processing circuit (figure 6) receives the interrupt request signal and the internal signal for generating the interrupt command and the interrupt vector identifying the interrupt service routine to be executed (column 5, lines 26 – 57).

With regard to claim 27, Oman et al. teach the additional limitation of a control circuit where a plurality of counters receives increment signals from a system clock signal (column 13, line 17, lines 35 – 37, lines 41 – 46).

With regard to claim 30, Khan et al. teach the additional limitation of a control circuit wherein the interrupts are nested, and wherein said logic processing circuit comprises:

A memory buffer coupled to said priority comparing circuit for storing the priority vale of the interrupt being represented by an internal signal (column 10, lines 52 – 64).

A stack register coupled to a memory buffer for storing the priority value corresponding to the interrupt service routine whose execution was stopped because of a new interrupt having a higher priority value (column 14, lines 58 – 64).

Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. in view of Chou et al, in view of Oman et al., and further in view of Farmer et al.

The system of Khan et al., as modified by both Chou et al. and Oman et al., discloses a plurality of counters that receive increment signals from a system clock signal or from externally generated timing signals. They fail to disclose the periodic nature of these signals. Farmer et al. teaches that a system may have a system clock which is divided into multiple other clocks and then distributed to the components of a system (column 1, lines 41 – 51). To produce a plurality of periodic signals generated from a multiple of the period of the system clock signal is well known and recognized in

the art. Therefore, to utilize the said signals in incrementing the said plurality of counters would have been obvious to one of ordinary skill in this art at the time of invention by applicant.

Claims 22, 23 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. in view of Chou et al., in view of Oman et al., and further in view of Norman et al.

With regard to claim 22, Khan et al., Chou et al., and Oman et al., fail to describe a control circuit wherein the increment signals have respective periods that are a multiple of a period of the system clock.

Norman et al. teach increment signals with respective periods that are based on a multiple of a period of the system clock signal (paragraph 91).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the control circuit of Khan et al., Chou et al., and Oman et al., to incorporate increment signals with respective periods that are a multiple of a period of the system clock signal in order

With regard to claim 23, Khan et al., and Oman et al. fail to teach incrementing each counter wherein the incrementing is based upon increment signals having different periods. Norman et al. teach incrementing priority values at different periods that may be fixed or variable (paragraphs 176, 182).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the method of Khan et al., and Oman et al., to incorporate the method of Norman et al. of incrementing the priority values of each interrupt according to different periods in order to provide a unique aging policy for each of said interrupts (paragraphs 176 – 178, 181 – 185).

With regard to claim 29, Khan et al., Oman et al., and Chou et al. fail to teach incrementing each counter wherein the incrementing is based upon increment signals having different periods. Norman et al. teach incrementing priority values at different periods that may be fixed or variable (paragraphs 176, 182).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the method of Khan et al., and Oman et al., to incorporate the method of Norman et al. of incrementing the priority values of each interrupt according to different periods in order to provide a unique aging policy for each of said interrupts (paragraphs 176 – 178, 181 – 185).

***Allowable Subject Matter***

Claims 12, and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Spittle whose telephone number is (571) 272-2467. The examiner can normally be reached on Monday - Friday, 8 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Cottingham can be reached on 571-272-7079. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MDS

JOHN R. COTTINGHAM
PRIMARY EXAMINER